

CLAIMS

1. A synchronous follow-up apparatus, comprising:
a PLL portion that outputs a first clock signal; and
a control loop portion that includes:

5 a reference frequency signal generating portion that outputs a reference frequency signal;

a clock signal generating portion that generates a second clock signal having the same frequency as a frequency of the first clock signal based on the reference frequency signal; and

10 a frequency control signal generating portion that generates a frequency control signal to change the frequency of the second clock signal based on a frequency difference between the first clock signal and the second clock signal that occurs after a predetermined time and outputs the frequency control signal to the clock signal generating portion.

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2. The synchronous follow-up apparatus as set forth in claim 1, wherein the PLL portion includes:

a voltage controlled oscillating portion that outputs an output signal as the first clock signal; and

20 a control voltage generating portion that detects a phase difference between a receiving signal and the output signal from the voltage controlled oscillating portion and generates a control voltage signal for inputting to the voltage controlled oscillating portion based on the phase difference.

- 25 3. The synchronous follow-up apparatus as set forth in claim 1, wherein

the PLL portion is an LSI having a PLL function.

4. The synchronous follow-up apparatus as set forth in claim 1, wherein the frequency control signal generating portion outputs a preceding frequency control signal which achieved a frequency tuning between the first clock signal and the second clock signal most recently when the detected frequency difference between the first clock signal and the second clock signal is equal to or greater than a predetermined value; and

wherein the clock signal generating portion outputs the second clock signal as a radio reference signal based on the frequency control signal output from the frequency control signal generating portion.

5. A synchronous follow-up method, comprising:

outputting a first clock signal from a PLL portion;

15 outputting a reference frequency signal;

generating a second clock signal having the same frequency as a frequency of the first clock signal based on the reference frequency signal;

detecting a frequency difference between the first clock signal and the second clock signal that occurs after a predetermined time;

20 generating a frequency control signal based on the frequency difference; and

outputting the frequency control signal to change the frequency of the second clock signal.

25 6. The synchronous follow-up method as set forth in claim 5, further

comprising:

outputting an output signal from a voltage controlled oscillating portion
as the first clock signal;

5 detecting a phase difference between a receiving signal and the output
signal; and

generating a control voltage signal based on the phase difference to
change the frequency of the output signal.

7. The synchronous follow-up method as set forth in claim 5, wherein, in
10 the generating process of the frequency control signal, a preceding frequency
control signal which achieved a frequency tuning between the first clock signal
and the second clock signal most recently is generated when the frequency
difference in the detecting process is equal to or greater than a predetermined
value; and

15 the synchronous follow-up method further comprises, outputting the
second clock signal as a radio reference signal based on the frequency control
signal.